RECORD OF TELEPHONIC INTERVIEW

On May 13, 2004, an interview was conducted with Primary Examiner Kenneth Wells. Both Andoh, et al. (U.S. 5.936,466) and Alexander, et al. (U.S. 5,936,469) were discussed with respect to the rejection of the Claims in the above-referenced Office Action. The Primary Examiner determined that Andoh did not anticipate Claim 18, but no agreement was reached with respect to the other independent claims or the Alexander reference. The Primary Examiner agreed that the reference signal of Andoh is not a data signal.

REMARKS

Claims 1-6 and 18-22 are currently pending in the application. Claims 16 and 17 were previously canceled and Claims 8-15 are currently withdrawn from prosecution.

1. Objections to the Specification

The Primary Examiner has objected to the specification, indicating informalities. The specification has been Amended to correct the informalities as indicated by the Primary Examiner. Therefore it is believed that the Primary Examiner's objections to the Specification have been overcome.

2. Objections to the Claims

The Primary Examiner has objected to claims 19-21, indicating informalities. Claims 19-21 have has been Amended to correct the informalities as indicated by the Primary Examiner. Therefore it is believed that the Primary Examiner's objections to the Claims have been overcome.

3. Rejections under 35 U.S.C. §102(b)

The Primary Examiner has rejected Claims 1 and 18-22 under 35 U.S.C. §102(b) as being anticipated by Andoh. Applicants respectfully disagree, but have Amended Claims 1 and 18 to more particularly point out features of the present invention. Amended Claim 1 recites a "receiver coupled to said first input, said second input and said third input for detecting a value of said single-ended data signal, said detected value representative of a digital binary state of said single-ended data signal, wherein detection of said value of said single-ended data signal is made in conformity with a common mode value of said differential data signal pair." Andoh does not disclose such a receiver for detecting a value corresponding to a binary state of a single-ended data signal in conformity with a differential pair common-mode value. Andoh discloses an op-amp (transconductance amp) that includes a feedback circuit having a reference voltage input. The Primary Examiner indicated in the above-referenced Office Action, that the gate of FET 11 of Andoh is read on by the first input

recited in Claim 1. Applicants respectfully point out that the indicated gate (input) is for connection of a DC reference voltage that is used to correct the output of the prior art op-amp disclosed in Andoh for the common-mode variation of the signal inputs of the op-amp. The feedback circuit 13 shown in Andoh does not detect a binary value of a single-ended data signal in conformity with a common mode value of a differential signal pair. Feedback circuit 13 does not receive a data signal input at all, and therefore does not detect a data signal in conformity with a common-mode voltage of a differential data signal pair. Therefore, Andoh does not disclose the interface of Claim 1, nor of dependent claims 2-6.

Similarly, Claim 18 recites "detecting a value of said single-ended data signal in conformity with a common-mode value of said received differential data signal pair, wherein said detected value is representative of a digital binary state of said single-ended data signal." As pointed out above, Andoh does not disclose a circuit for performing such detection, and therefore does not disclose the method recited in Claim 18, nor dependent Claim 19-22.

The Primary Examiner has also indicated that Alexander appears to anticipate at least independent Claims 1 and 18 as well. Applicants respectfully disagree. For the same reasons stated above with respect to Andoh, Alexander does not teach a detector as recited in Claim 1 or the detecting step recited in

Claim 18, as the circuits disclosed in Andoh are likewise op-amps having a common mode compensation input and not detectors for detecting the binary state of a single-ended signal in conformity with a common-mode value of a differential signal pair. Applicants believe that the rejection under 35 U.S.C. §102(b) has been overcome.

Therefore, for all of the reasons stated above, applicants believe that all of the rejections and objections have been overcome.

CONCLUSION

In conclusion, Applicants respectfully submit that this Amendment, in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Primary Examiner in the Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 1-6 and 18-22 are in condition for allowance. Such action is earnestly solicited. Should a Notice of Allowance be issued, it is requested that the Primary Examiner further allow previously withdrawn Claims 7-12, which depend from Claim 1 and should be found allowable if Claim 1 is allowed.

No fees should be incurred by this Amendment, but if there are any fees incurred by this Amendment, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully submitted,

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